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(54) Semiconductor device in which wiring layer is formed below bonding pad.

(57) In a semiconductor device wherein a bonding pad (22 or 23) is formed on an electrode (17-1 to 17-8, or 18-1 to 18-8) through an insulating interlayer (19) and a bonding wire (25 or 26) is bonded to the bonding pad (22 or 23) by thermocompression bonding, a through hole (21-1 to 21-4, or 20-1 to 20-3) for connecting the bonding pad (23 or 22) and the electrode (17-4 to 17-7, or 18-1 to 18-3) is formed in the insulating interlayer (19) above a contact hole (15-1 to 15-7, or 16-1 to 16-8) for connecting the electrode (17-1 to 17-8, or 18-1 to 18-8) and an active region (13-1 to 13-7, or 12) formed in a semiconductor substrate (11). Metal columns of members of the electrode (17-4 to 17-7, or 18-1 to 18-3) filled in the contact hole (15-4 to 15-7, or 16-1 to 16-3) and members of the bonding pad (23 or 22) filled in the through hole (20-1 to 20-3, or 21-1 to 21-4) are formed under the bonding pad (23 or 22).

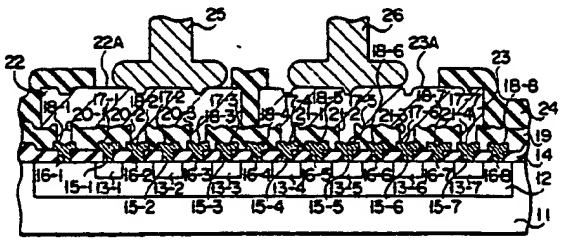

FIG. 1

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Semiconductor device in which wiring layer is formed below bonding pad

The present invention relates to a semiconductor device in which a second wiring metal layer is formed on a first metal wiring layer through an insulating interlayer and wire bonding is performed for the second metal wiring layer and, more particularly, to prevention of cracking of the insulating interlayer formed immediately below a bonding region.

In a conventional bipolar transistor, an emitter region is formed in a comb-like shape in order to reduce an output capacitance, improve high-frequency characteristics, and satisfy a need for increasing an output capacity. The emitter region is formed in a surface part of a base region. The base region is formed in a major surface region of a semiconductor substrate which serves as a collector region. A comb-like emitter electrode is formed on the emitter region so as to correspond to the emitter region. A comb-like base electrode is formed on the base region. The emitter and base electrodes are formed such that teeth of the electrodes are arranged in an interdigital manner at predetermined intervals.

In order to effectively utilize an active region of a transistor, a multilayered structure is utilized in which bonding pads are formed on the emitter and base electrodes through an insulating interlayer. In this case, base and emitter bonding pads are used. The base bonding pad is connected to part of the base electrode through a contact hole formed in the insulating interlayer. The emitter bonding pad is connected to part of the emitter electrode through another contact hole formed in the insulating interlayer. Base and emitter deriving bonding wires are respectively bonded to the bonding pads by thermocompression bonding.

With the above arrangement, the active region can be effectively utilized, and resistances from the emitter and base regions to the corresponding bonding wires can be reduced. In addition, the dynamic characteristics of the transistor can also be improved.

With the above arrangement, however, mechanical stress acts on the insulating interlayer by a pressure during bonding of base and emitter deriving bonding wires. The insulating interlayer is formed on the interdigital base and emitter electrodes, i.e., a portion having a large three-dimensional pattern. Therefore, a three-dimensional portion is formed on the surface of the insulating interlay r accordingly. A bonding pressure tends to be concentrated on a step of the three-dimensional pattern on the surface of the insulating interlayer. For this reason, a crack tends to occur in the insulating interlayer. In the worst case, the insulating interlayer is destroyed. Such a crack cannot be easily found by an initial electrical function test. Therefore, reliability of the semiconductor device is undesirably degraded.

It is, therefore, an object of the present invention to provide a semiconductor device wherein cracking of an insulating interlayer formed immediately under a bonding region can be suppressed, and reliability of the semiconductor device can be improved.

According to an embodiment of the present invention, there is provided a semiconductor device comprising: a semiconductor substrate; an activ region formed in a region of a major surface of the semiconductor substrate; a first insulating layer formed on the major surface of the semiconductor substrate which includes the active region; a first contact hole formed at a position in the first insulating layer corresponding to the active region; a first conductive layer formed in the first contact hol and a portion of the first insulating layer around the contact hole; a second insulating layer formed on the first conductive layer and the first insulating layer; a second contact hole formed at a position in the second insulating layer corresponding to the first conductive layer and located above the first contact hole; a second conductive layer formed on the second insulating layer and filled in the second contact hole; and a bonding wire connected to the second conductive layer in regions located above the first and second contact holes.

With the above structure, the pressure applied to the second insulating layer during wire bonding can be supported by columnar portions of the first and second conductive layers filled in the first and second contact holes. Therefore, the pressure acting on the second insulating layer can be reduced to suppress occurrence of cracks, thereby providing a highly reliable semiconductor device.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a sectional view of a semiconductor device according to an embodiment of the present invention; and

Fig. 2 is a plan view showing a pattern of the semiconductor device shown in Fig. 1.

Fig. 1 is a sectional view of a semiconductor device according to an embodiment of the pres nt invention. Fig. 2 is a plan view showing a pattern of the semiconductor device shown in Fig. 1, when taken along the line X - X′ of Fig. 1. Figs. 1 and 2 ex mplify an npn bipolar transistor as a semiconductor device having a wiring layer under the bond-

ing pad. N-type semiconductor substrate (silicon substrate 11 serves as a collector region. P-type base region 12 is formed in the major surface region of semiconductor substrate 13. N-type emitter region 13 is formed in a surface region of base region 12. Emitter region 13 has comb-like teeth 13-1 to 13-7. 3,000-Å thick first insulating layer 14 is formed on the major surface of semiconductor substrate 11. Contact hole 15 is formed by photoetching at a position in first insulating layer 14 corresponding to emitter region 13. Contact hole 15 has a shape corresponding to emitter region 13. Contact hole 16 is formed by photoetching at a position in first insulating layer 14 corresponding to base region 12. Contact hole 16 has a shape corresponding to base region 12. Emitter electrode 17 is filled in contact hole 15 and formed on first insulating layer 14 around contact hole 15. Base electrode 18 is filled in contact hole 16 and is formed on first insulating layer 14 around contact hole 16. Emitter and base electrodes 17 and 16 are formed interdigitally. Teeth 17-1 to 17-7 and teeth 18-1 to 18-8 are interdigitally formed at predetermined intervals. Emitter electrode 17 and base electrode 18 are formed such that a 1-μm thick aluminum film or an aluminum alloy film deposited on first insulating layer 14 is patterned by photoetching. Emitter electrode 17 filled in contact hole 15 is brought into ohmic contact with emitter region 13. Base electrode 18 filled in contact hole 16 is brought into ohmic contact with base region 12. 2-μm thick second insulating layer 19 is formed on emitter electrode 17, base electrode 16, and first insulating layer 14. Second insulating layer 19 comprises an insulating interlayer of SiO_2 or Si_3N_4 formed by plasma CVD. Contact holes 20-1 to 20-3 are formed at positions in second insulating layer 19 respectively corresponding to teeth 18-1 to 18-3 of base electrode 18. Contact holes 21-1 to 21-4 are formed at positions in second insulating layer 19 respectively corresponding to teeth 17-4 to 17-7 of emitter electrode 17. Base bonding pad 22 is formed on second insulating layer 19 and filled in contact holes 20-1 to 20-3. Emitter bonding pad 23 is formed on second insulating layer 19 and filled in contact holes 21-1 to 21-4. Bonding pads 22 and 23 are formed such that a 3-μm thick aluminum film or aluminum alloy film is deposited on the second insulating layer and is patterned by photoetching.

Members of base bonding pad 22 filled in contact holes 20-1 to 20-3 are respectively connected to base electrodes 16-1 to 16-3. Members of emitter bonding pad 23 filled in contact holes 21-1 to 21-4 are respectively connected to emitter electrodes 17-4 to 17-7. Passivation film 24 is formed on the resultant structure except for bonding portions 22A and 23A of bonding pads 22 and 23. Base d riving bonding wire 25 is formed on bonding portion 22A by thermocompression bonding. Emitter deriving bonding wire 26 is formed on bonding portion 23A by thermocompression bonding. Ball bonding (this method is also called as nailhead bonding) is performed for bonding bonding wires 25 and 26 by thermocompression bonding. Gold wires are used as bonding wires 25 and 26.

With the above structure, two metal columns are formed under bonding portion 22A. One metal column consists of aluminum of bonding pad 22 filled in contact hole 20-2 and aluminum of base electrode 18-2 filled in contact hole 16-2. The other metal column consists of aluminum of bonding pad 22 filled in contact hole 20-3 and aluminum of base electrode 18-3 filled in contact hole 16-3. Thes metal columns receive part of the pressure applied to bonding pad 22 during thermocompression bonding of bonding wire 25. Similarly, a m tal column is also formed under bonding portion 23A. This metal column consists of aluminum of bonding pad 23 filled in contact hole 21-2 and aluminum of emitter electrode 17-5 filled in contact hole 15-5. The metal column receives part of the pressure acting on bonding pad 23 during thermocompression bonding of bonding wire 26. Therefore, the pressure acting on insulating interlayer 19 can be reduced, and formation of cracks in the step of insulating interlayer 19 can be prevented.

Portions where the metal columns are formed, i.e., the contact portion between bonding pad 22 and teeth 18-1 to 18-3 of base electrode 18 and the contact portion between bonding pad 23 and teeth 17-4 to 17-7 of emitter electrode 17 are preferably formed to cover the entire active region. Then, formation of cracks of insulating interlayer 19 can be suppressed with best efficiency. A wiring resistance from base region 12 to base deriving bonding wire 25 and a wiring resistance from emitter region 13 to emitter deriving bonding wire 26 can also be reduced. However, contact holes may be formed such that the metal columns are formed under only bonding portions 22A and 23A bonded to bonding wires 25 and 26.

The present inventor examined the frequency of occurrence of cracks of the insulating interlayer of the semiconductor device (Figs. 1 and 2) of the present invention and that of the conventional semiconductor device. The materials and thicknesses of base and emitter electrodes, the material and thickness of the first insulating layer, and the material and thickness of the insulating interlayer were identical in the device of the present invention and the conventional device. As a result, the frequency of occurrence of cracks of the insulating interlayer in the conventional semiconductor device was 60% (12/20 devices), while that of the semi-

conductor device of the present invention was 15% (3/20 devices). As is apparent from this result, the frequency of occurrence of cracks of the insulating interlayer according to the present invention could be confirmed to be greatly reduced as compared with the conventional semiconductor device. When a defective (cracked) semiconductor device was examined with a microscopic picture, cracks in the insulating interlayer were concentrated on the corner portion of the emitter or base electrode pattern. Therefore, these cracks can be assumed to be formed by concentration of stress during bonding.

The above embodiment exemplifies an npn bipolar transistor. However, the present invention is not limited to this type of transistor. The present invention is applicable to a pnp bipolar transistor or any other semiconductor device. In the above embodiment, bonding pads 22 and 23 are formed on insulating interlayer 19. However, the present invention is further applicable to a multilayered wiring structure wherein an insulating interlayer is formed on the first wiring layer and the second wiring layer is formed on the insulating interlayer if the semiconductor device allows bonding of the second wiring layer.

Claims

1. A semiconductor device comprising a semiconductor substrate (11), an active region (12 or 13) formed in a region of a major surface of said semiconductor substrate (11), a first insulating layer (14) formed on said major surface of said semiconductor substrate (11), a first contact hole (15 or 16) formed at a position in said first insulating layer (14) corresponding to said active region (12 or 13), a first conductive layer (17 or 18) formed in said first contact hole (15 or 16) and a portion of said first insulating layer (14) around said contact hole (15 or 16), a second insulating layer (19) formed on said first conductive layer (17 or 18) and said first insulating layer (14), a second contact hole (20-1 to 20-3, or 21-1 to 21-4) formed at a position in said second insulating layer (19) corresponding to said first conductive layer (17 or 18), a second conductive layer (22 or 23) formed on a portion of said second insulating layer (19) and filled in said second contact hole (20-1 to 20-3, or 21-1 to 21-4), and a bonding wire (25 or 26) connected to said second conductive layer (22 or 23),

characterized in that said second contact hole (20-1 to 20-3, or 21-1 to 21-4) is located above said first contact hole (15 or 16), said bonding wir (25 or 26) is bonded on regions of said second conductive layer (22 or 23) at positions above said first and second contact holes (15 or 16; 20-1 to 20-3, or 21-1 to 21-4), and portions of said first conductive lay r (17 or 18) filled in said first contact hole (15 or 16) and said second conductiv layer (22 or 23) fill d in said second contact hole receive part of a pressure which is caused by a pressure applied to said conductive layer (22 or 23) during wire bonding and which acts on said second insulating layer (19).

2. A device according to claim 1, characterized in that said active region includes a first impurity region (12) formed in said region of said major surface of said semiconductor substrate (11) and having a conductivity type opposite to that of said semiconductor substrate (11) and a second impurity region (13) formed in a surface portion of said first impurity region (12) and having the same conductivity type as that of said semiconductor substrate (11).

3. A device according to claim 2, characterized in that said first contact hole (15) is formed in a portion of said first insulating layer (14) on said second impurity region (12), and said first conductive layer (17) is filled in said first contact hole (15) and formed on said first insulating layer (14) around said first contact hole (15).

4. A device according to claim 2, characterized in that said first contact hole (16) is formed in a portion of said first insulating layer (14) on said first impurity region (12), and said first conductive layer (18) is filled in said first contact hole (16) and formed on said first insulating layer (14) around said first contact hole (16).

5. A device according to claim 2, characterized in that said semiconductor substrate (11) serves as a collector region, said first impurity region (12) serves as a base region, and said second impurity region (13) has a comb-like shape and serves as an emitter region.

6. A device according to claim 5, characterized in that said first conductive layer includes a comb-like emitter electrode (17) and a comb-like base electrode (18), said column-like emitter and base electrodes (17, 18) being arranged such that teeth (17-1 to 17-7) of said emitter electrode (17) and teeth (18-1 to 18-8) of said base electrode (18) are interdigitally arranged at predetermined intervals.

7. A device according to claim 1, characterized in that said second insulating layer includes an insulating interlayer (19).

8. A device according to claim 1, characterized in that said second conductive layer includes a bonding pad (22 or 23).

9. A device according to claim 8, characterized in that said bonding wire (25 or 26) is bonded to said bonding pad (22 or 23) by thermocompression bonding.

10. A semiconductor device including a second wiring layer formed on a first wiring layer through an insulating layer and a bonding wire formed on

said second wiring layer, characterized by comprising a semiconductor region (11 or 12) of a first conductivity type, an impurity region (12 or 13) formed in a major surface portion of said semiconductor region (11 or 12) and having a second conductivity type, a first insulating layer (14) formed on said semiconductor region (11 or 12), a first contact hole (12 or 13) formed at a position in said first insulating layer (14) corresponding to said impurity region (12 or 13) of the second conductivity type, a first wiring layer (17 or 18) filled in said first contact hole (15 or 16) and formed on said first insulating layer (14) around said first contact hole (15 or 16), a second insulating layer (19) formed on said first wiring layer (17 or 18) and said first insulating layer (14), a second contact hole (20-1 to 20-3, or 21-1 to 21-4) formed at a position in said second insulating layer (19) corresponding to said first wiring layer (17 or 18), a second wiring layer (22 or 23) filled in said second contact hole (20-1 to 20-3, or 21-1 to 21-4) and formed on said second insulating layer (19), and a bonding wire connected to said second wiring layer (22 or 23),

wherein portions of said first wiring layer (17 or 18) filled in said first contact hole (15 or 16) and said second wiring layer (22 or 23) filled in said second contact hole (20-1 to 20-3, or 21-1 to 21-4) receive a pressure which is caused by a pressure applied to said second wiring layer (22 or 23) during bonding of said bonding wire (25 or 26) to said second wiring layer (22 or 23) and which acts on said second insulating layer (19).

11. A device according to claim 10, characterized in that said first conductive layer includes a comb-like emitter electrode (17) and a comb-like base electrode (18), said column-like emitter and base electrodes (17, 18) being arranged such that teeth (17-1 to 17-7) of said emitter electrode (17) and teeth (18-1 to 18-8) of said base electrode (18) are interdigitally arranged at predetermined intervals.

12. A device according to claim 10, characterized in that said second insulating layer includes an insulating interlayer (19).

13. A device according to claim 10, characterized in that said second conductive layer includes a bonding pad (22 or 23).

14. A device according to claim 13, characterized in that said bonding wire (25 or 26) is bonded to said bonding pad (22 or 23) by thermocompression bonding.

15. A semiconductor device including a bonding pad formed on an electrode through an insulating layer, characterized by comprising a semiconductor substrate (11) of a first conductivity type, a first impurity region (12) formed in a major surface portion of said semiconductor substrate (11) and having a second conductivity type, a comb-like second impurity region (13) formed in a surface lay r of said first impurity region (12) and having the first conductivity type, a first insulating layer (14) formed on said semiconductor substrate (11), a first contact hole (15) formed at a position in said first insulating layer (14) corresponding to said second impurity region (13), a second contact hole (16) formed at a position in said first insulating layer (14) corresponding to said first impurity region (12), a comb-like first electrode (17) filled in said first contact hole (15) and formed on said first insulating layer (14) around said first contact hole (15), a comb-like second electrode (18) filled in said second contact hole (16) and formed on said first insulating layer (14) around said second contact hole (16), a second insulating layer (19) formed on said first and second electrodes (17 and 18) and said first insulating layer (14), a third contact hole (21-1 to 21-4) formed at a position in said second insulating layer (19) partially corresponding to said first electrode (17), a fourth contact hole (20-1 to 20-3) formed at a position in said second insulating layer (19) partially corresponding to said second electrode (18), a first bonding pad (23) filled in said third contact hole (21-1 to 21-4) and formed on a portion of said second insulating layer (19), a second bonding pad (22) filled in said fourth contact hole (20-1 to 20-3) and formed on a portion of said second insulating layer (19), a first bonding wire (26) connected to said first bonding pad (23), and a second bonding wire (25) connected to said second bonding pad (22),

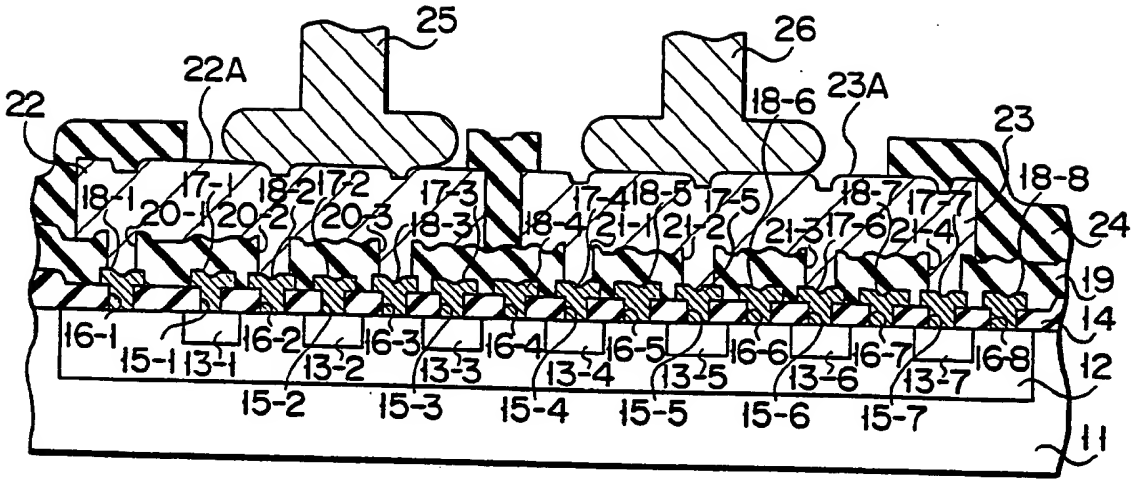
wherein a first portions of a member of said first electrode (17) filled in said first contact hol (16) and a member of said first bonding pad (23) filled in said third contact hole (21-1 to 21-4) receive part of a pressure which is caused by a pressure applied to said first bonding pad (23) during bonding of said first bonding wire (26) to said bonding pad (23) and which acts on said second insulating layer (19), and second portions of members of said second electrode (16) filled in said second contact hole (15) and members of said second bonding pad (22) filled in said fourth contact hole (20-1 to 20-3) receive part of a pressure which is caused by a pressure applied to said second bonding pad (22) during bonding of said second bonding wire (25) to said first bonding pad (22) and which acts on said second insulating layer (19).

16. A device according to claim 15, characterized in that said first electrode includes an emitt r electrode (17).

17. A device according to claim 15, characterized in that said second electrode includes a base electrode (18).

18. A device according to claim 15, characterized in that said second insulating layer includes an insulating interlay r (19).

19. A device according to claim 15, characterized in that said first and second bonding wires (25 and 26) are respectively bonded to said first and second bonding pads (22 and 23) by thermocompression bonding.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26
22A
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23A
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18-8
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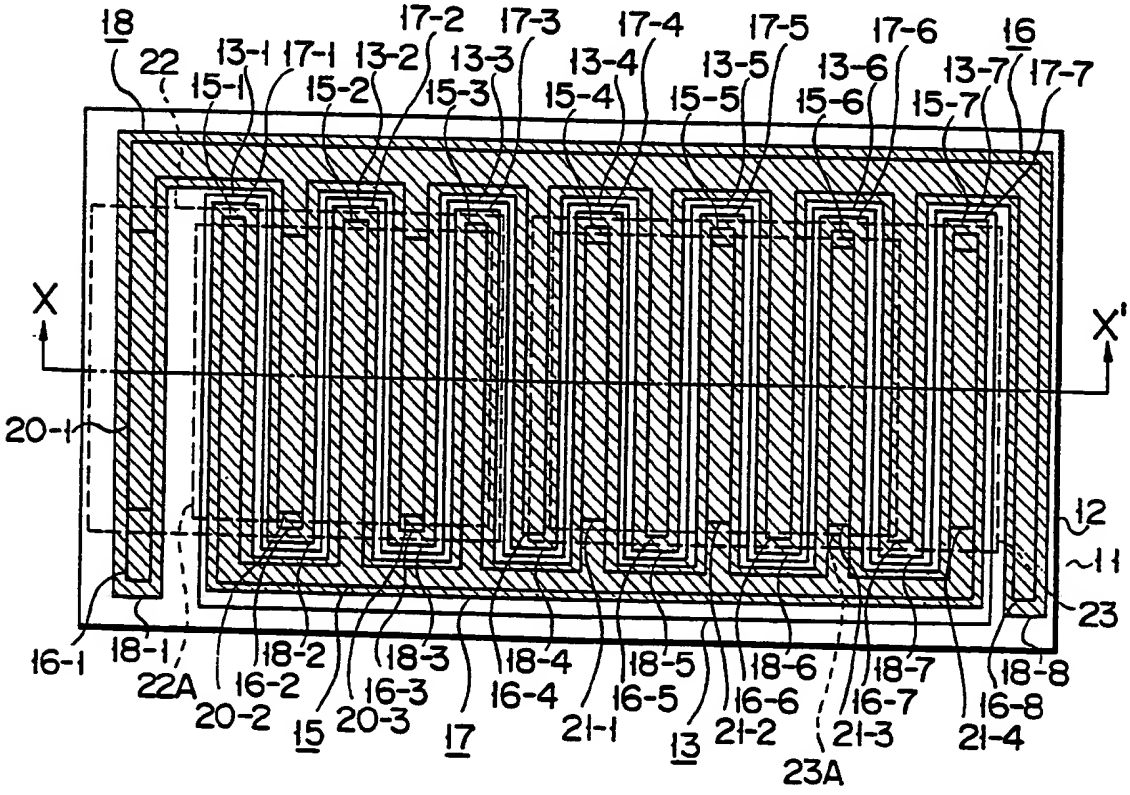
FIG. 1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21-2
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23A
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18-7
16-8
21-4
18-8

FIG. 2

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(54) **Semiconductor device in which wiring layer is formed below bonding pad.**

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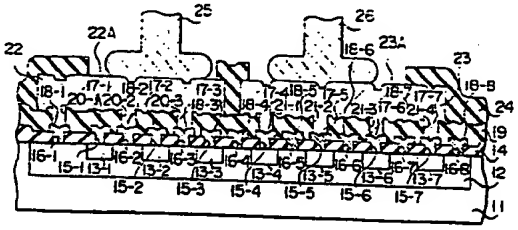

FIG. 1

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EUROPEAN SEARCH REPORT

Application Number

EP 88 10 7501

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
A	EP-A-0 100 100 (K.K. TOSHIBA) * Abstract; page 4, lines 1-31; claim 1; figure 2 *	1,2,8-10,13-17,19	H 01 L 23/48
A	IEDM INTERNATIONAL ELECTRON DEVICES MEETING, 7th-9th December 1981, pages 62-65, IEEE, Washington, D.C., US; K. MUKAI et al.: "A new integration technology that enables forming bonding pads on active areas" * Page 62, "Abstract"; pages 62-63, "Film strength"; figure 2 *	1,8-10, 13-15, 19	

TECHNICAL FIELDS SEARCHED (Int. Cl.4)

H 01 L 23/00
H 01 L 21/00

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	19-04-1989	DELPORTE B.P.M.

CATEGORY OF CITED DOCUMENTS

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